IN THE CLAIMS

Replace the claims with the following:

1. (Currently Amended) A device for reading a cell (4) of a memory, ~~including~~ comprising:

a differential sense amplifier (18) having a first input terminal (16) connected to a cell column (10); and

a circuit (34) [[intended to provide]] for providing to a second input terminal (20) of the amplifier (18) a reference voltage (Vref), wherein said circuit (34) [[includes]] comprises:

a first means (38) for storing the voltage of said column; and

a second means (~~38~~, 40, 42) for applying as [[a]] the reference voltage (Vref) the stored voltage modified by a predetermined amount.

2. (Currently Amended) The device of claim 1, wherein the presence of a cell translates as a reduction in the voltage of a column [[and characterized in that]] wherein the reference voltage is reduced by a predetermined amount with respect to the stored voltage.

3. (Currently Amended) The device of claim 1, wherein said [[circuit (34) includes]] first means is a first capacitive element (38) ~~intended to store the~~ for storing a precharge voltage (Vpch) and the second means is a second capacitive element (40) connectable in parallel [[on]] with the first ~~one~~ capacitor to set the value of the reference voltage (Vref).

4. (Original) The device of claim 3, wherein the capacitive elements are formed of the gate-source, gate-substrate, and gate-drain capacitances of MOS transistors.

5. (Currently Amended) The device of claim 1, wherein each column is associated with a precharge transistor (12) [[and in that]] , wherein the precharge transistors are addressable independently.

6. (Currently Amended) A method for reading a cell (4) of a memory, ~~including~~ comprising the steps of:

storing the voltage of a column just before reading; and

modifying the stored voltage by a predetermined amount and using the modified voltage as a reference voltage.

7. (Currently Amended) The ~~read~~ method of claim 6, further ~~consisting~~ comprising the step of comparing the reference voltage with a column voltage.

8. (Currently Amended) The ~~reading~~ method of claim 6, ~~including~~ further comprising the steps of:

applying [[the]] a precharge voltage (Vpch) on a first capacitor (38);

disconnecting the first capacitor from the precharge voltage; and

connecting in parallel [[on]] with the first capacitor a second capacitor (40).